In the Claims:

1. (Original) A method of reducing the circuit failure caused by tungsten plug pulling out of an apparatus comprising the steps of:

providing a substrate having a lower portion and a layer of selected material over said lower portion, said selected material having a top surface;

defining an aperture in said selected material extending from said top surface toward said lower portion;

depositing a layer of tungsten over said top surface of said layer of selected material, said tungsten also filling said aperture;

polishing said tungsten layer to remove a top portion of said tungsten layer;

stopping said polishing so as to leave a reduced thickness of said tungsten layer; and

providing a contact area over at least a portion of said tungsten filled aperture, said contact area in electrical contact with said tungsten filling said aperture.

2. (Original) The method of claim 1 wherein said aperture is a trench.

3. (Original) The method of claim 1 wherein said substrate further includes a conductive area covered by said layer of selected material and wherein said aperture is a via extending through said layer of selected material and said tungsten in said via is in electrical contact with said conductive area.

4. (Original) The method of claim 1 wherein said reduced layer of tungsten remaining after polishing is between 0.3 μm and 0.01 μm.

5. (Original) The method of claim 1 wherein said layer of selected material is one of a layer of a dielectric material and a layer of insulating material.

6. (Original) The method of claim 1 further comprising the step of depositing a liner material in said aperture and over said top surface of said selected material before depositing said layer of tungsten.

7. (Original) The method of claim 3 wherein said contact area is made of a conductive material selected from the group consisting of copper, aluminum and an alloy of copper and aluminum.

8. (Original) The method of claim 3 wherein said conductive area is made of a conductive material selected from the group consisting of copper, aluminum and an alloy of copper and aluminum.

9. (Original) The method of claim 8 wherein said contact area is made of a conductive material selected from the group consisting of copper, aluminum and an alloy of copper and aluminum.

10. (Original) The method of claim 6 wherein said liner material is selected from the group consisting of tantalum, tantalum nitride, titanium, and titanium nitride.

Please cancel Claims 11-20.

21. (New) A method of reducing integrated circuit failures in an integrated circuit chip caused by metal plug pull-ups and pull-outs while making said chip, said method comprising:

forming an aperture in a top surface of a selected material layer, said selected material layer being formed over a wafer, wherein said aperture extends toward said wafer from said top surface;

depositing a layer of metal over said top surface of said selected material layer and into said aperture to fill said aperture with metal;

polishing said metal layer to remove a top portion of said metal layer;

stopping said polishing to leave a reduced thickness portion of said metal layer adjacent to said aperture;

forming a contact pad at least partially over said metal filled aperture; and

removing at least part of said reduced thickness portion of said metal layer during said forming of said contact pad.

22. (New) The method of claim 21, wherein the metal comprises tungsten.

23. (New) The method of claim 21 wherein said reduced thickness portion of said metal layer has a thickness between about 0.3 μm and 0.01 μm.

24. (New) The method of claim 21 wherein said wafer has a diameter greater than 200 mm.

25. (New) The method of claim 21 wherein said selected material layer comprises a dielectric material.

26. (New) The method of claim 21 further comprising:

depositing a liner material layer in said aperture and over said top surface of said selected material layer before depositing said metal layer, wherein said metal layer is formed over said liner material layer.

27. (New) A method of making an integrated circuit chip, the method comprising:

forming an aperture in a top surface of a selected material layer, said selected material layer being formed over a wafer, wherein said aperture extends toward said wafer from said top surface;

depositing a layer of metal over said top surface of said selected material layer and into said aperture to fill said aperture with metal;

polishing said metal layer to remove a top portion of said metal layer;

stopping said polishing to leave a reduced thickness portion of said metal layer adjacent to said aperture;

forming a contact pad at least partially over said metal filled aperture; and

removing at least part of said reduced thickness portion of said metal layer during said forming of said contact pad.

28. (New) The method of claim 27, wherein the metal comprises tungsten.

29. (New) The method of claim 27 wherein said reduced thickness portion of said metal layer has a thickness between about 0.3 μm and 0.01 μm.

30. (New) The method of claim 27 wherein said wafer has a diameter greater than 200 mm.

31. (New) The method of claim 27 wherein said selected material layer comprises a dielectric material.

32. (New) The method of claim 27 further comprising:

depositing a liner material layer in said aperture and over said top surface of said selected material layer before depositing said metal layer, wherein said metal layer is formed over said liner material layer.